REMARKS

In view of the preceding amendments and following remarks, reconsideration of the present application is respectfully requested.

Claims 1-4 were pending in the Application and were rejected. By this Response, Claims 1-4 are canceled, and Claims 6-8 are added. A formal drawing for the only figure, Fig. 1, is also included herein as a replacement sheet. A new Abstract is also submitted herein. No new matter is introduced herein.

Claims 1-4 were rejected under 35 USC 103(a) as being unpatentable over Leyrer in view of Cohen, et al. Claims 1-4 were broadly worded and apparently were obvious in view of the cited prior art.

Claims 1-4 are canceled herein in order to present more clearly worded and more precisely constructed, narrower subject matter Claims 6-8. Claims 1-4 included processors, cache memry, power supply switches and connections, etc. Claims 6-8 are drafted to recite the subject matter of cache interface ciruit (14) of Fig. 1.

The Abstract is rewritten to also describe the cache interface ciruit (14). The Title is rewritten to reflect the claimed subject matter.

A cache interface circuit embodiment of the present invention includes a processor interface for receiving memory access requests from a processor, and for transmitting memory data back to the processor in response to processor requests. Specification page 2, lines 25-26. A main memory interface provides for issuing main memory access requests to a main memory and for receiving main memory data in response. Specification page 2, lines 26-28. A cache memory interface provides for issuing memory access requests to a cache memory, if operating in a cache mode, and for receiving cache memory data in response. Specification page 2, lines 26-28, and page 3, lines 1-14. A cache-bypass mode-control signal input provides for the processor to indicate a cache-bypass mode in which memory access requests are serviced from the main memory. Specification page 3, line 29, to page 4, line 3. A power control output provides for switching off operating power to the cache memory in response to a command received at the cache-bypass mode-control signal input that indicates all memory access requests should be serviced from the main memory. Specification page 2, line 28, and page 3, lines 23-28.

Claims 7-8 recite the subject matter disclosed by the Specification at page 4, lines 3-8. Claim 8 recites subject matter disclosed by the Specification at page 4, lines 9-31.

In contrast to the cited prior art, the claimed present invention does not depend on timers to control whether a power saving power-down of the cach memory is to occur. The Office Action cited Cohen, et al., at column 17, lines 55-59. But such does not teach how one would detect "periods of time when the master cache is not being addressed" nor how the "power-down mode" would be implemented. Claims 6-8 are very specific. The Office Action further cited Leyrer, Abstract, and Figs. 4, 6. Such reference, in its Abstract and column 4, lines 47-58, mentions cache inhibiting signals. But such are described as being operated for non-cacheable areas, e.g., video memory. Not for power savings.

Accordingly, in view of the preceding amendments and remarks, it is respectfully submitted that the pending application, with pending claims 6-8, is in condition for allowance and such action is respectfully requested.

Should the Examiner be of the opinion that a telephone conference with Applicant's attorney would expedite matters, the Examiner is invited to contact the undersigned.

Respectfully submitted,

Dated: March 16, 2004

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